CLAIMS

1. A CMOS bus hold circuit defining an input and an output, the bus hold circuit powered from a positive power rail, Vcc, the bus hold circuit comprising:

a first inverter receiving an input signal, Vin, at the input and providing its complement at the output,

an arbiter circuit arranged to selectively connect the more positive of Vin or Vcc to a pseudo power rail or prail,

a second inverter receiving the output and providing its complement back to the input thereby latching or holding the logic state of Vin, the second inverter defining a power connection,

a PMOS transistor arranged, when on, to connect the power connection to Vcc, and when off to disconnect the second inverter from Vcc, thereby allowing the power connection to float, and where the PMOS N-well is connected to the prail, thereby preventing the PMOS drain to N-well from being forward biased,

a comparator circuit arranged to receive and compare Vin to Vcc, and provide a control signal equal to Vin when the Vin is higher than Vcc, and to disconnect the control signal, allowing it to float, when Vcc is higher than Vin, and

a switch that is on and pulls the control signal low when Vin is a logic low, and where the switch is off when Vin is not a logic low,

wherein the bus hold circuit draws no DC current, and where when Vin is higher than Vcc no leakage current is drawn from Vin.

2. The bus hold circuit of claim 1 wherein the arbiter circuit comprises two PMOS transistors with their drains and N-wells connected together.

3. The bus hold circuit of claim 1 wherein the switch is a PMOS transistor with its gate connected to Vin and its source connected to the control signal.

4. The bus hold circuit of Claim 1 wherein the comparator comprises:

a first PMOS with its source connected to Vin and its gate connected to Vcc,

a second PMOS with its source connected to the drain of the first PMOS and its gate connected to Vcc, and its drain connected to the control signal,

a third PMOS with its source connected to the source of the second PMOS and its gate connected to Vin,

wherein the N-wells of the first, second, and third PMOS transistors are all connected to the prail,

a first NMOS with its drain connected to the drain of the second PMOS and its source connected to a power return,

a second NMOS with its drain connected to the drain of the third PMOS, its gate connected to its drain and to the gate of the first NMOS, and its source connected to the power return, wherein the first, second, and third PMOS transistors and the first and second NMOS transistors form a comparator circuit wherein the control signal is connected to Vin when Vin is higher the Vcc, and where the control signal is unconnected and floats when Vcc is higher than Vin, and further wherein the comparator uncertainty when Vin and Vcc are near each other is limited to differential of about 100 millivolts.

5. A bus hold circuit defining an input and an output, the bus hold circuit powered from a positive power rail, Vcc, the bus hold circuit comprising:

means for receiving an input signal, Vin, at the input and providing its complement at the output,

means to selectively connect the more positive of Vin or Vcc to a pseudo power rail or prail,

inverter means for receiving the output and providing its complement back to the input thereby latching or holding the logic state of Vin,

means for connecting and disconnecting the inverter means to Vcc, wherein when disconnected the inverter means floats,

means for comparing Vin to Vcc, and for providing a control signal equal to Vin when the Vin is higher than Vcc, and for disconnecting the control signal, allowing it to float, when Vcc is higher than Vin, and

means for pulling the control signal low when Vin is a logic low,

wherein the bus hold circuit. draws no DC current, and when Vin is higher than Vcc no leakage current is drawn from Vin.

6. A process for holding an input bus signal and outputting the signal or its complement, the process comprising the steps of:

receiving an input signal, Vin, at an input and providing its complement,

selectively connect the more positive of Vin or Vcc to a pseudo power rail or prail,

receiving the output and providing its complement back to the input thereby defining an inverter for latching or holding the logic state of Vin,

connecting and disconnecting the inverter to Vcc, wherein when disconnected the inverter means floats,

comparing Vin to Vcc, and providing a control signal equal to Vin when the Vin is higher than Vcc, and for disconnecting the control signal, allowing it to float, when Vcc is higher than Vin, and

pulling the control signal low when Vin is a logic low,

configuring the process to draw no DC current and no leakage current when Vin is higher than Vcc.

7. A computer system including one or more of the bus hold circuits defined in Claim 1.